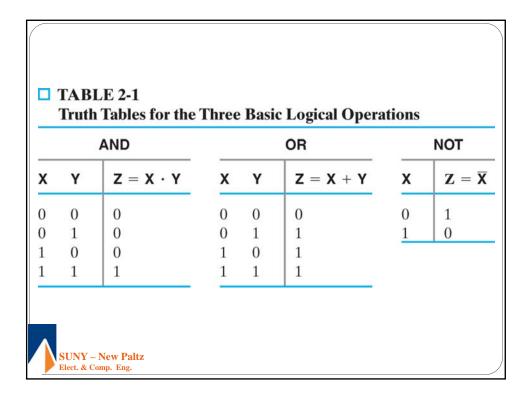


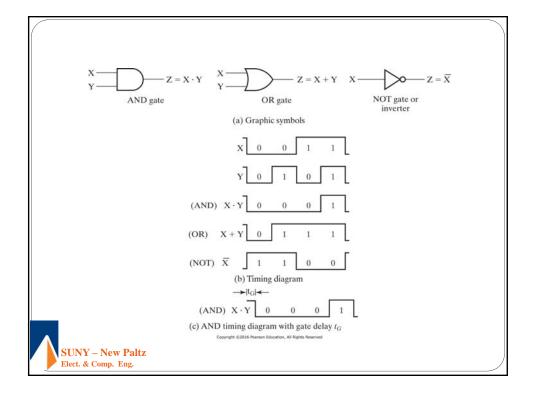
Decimal (base 10)	Binary (base 2)	Octal (base 8)	Hexadecimal (base 16)
00	0000	00	0
01	0001	01	1
02	0010	02	2
03	0011	03	3
04	0100	04	4
05	0101	05	5
06	0110	06	6
07	0111	07	7
08	1000	10	8
09	1001	11	9
10	1010	12	A
11	1011	13	В
12	1100	14	C
13	1101	15	D
14	1110	16	E
15	1111	17	F

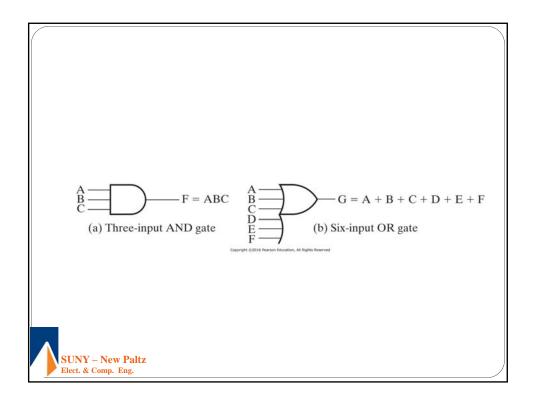
Decimal	BCD
Symbol	Digit
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

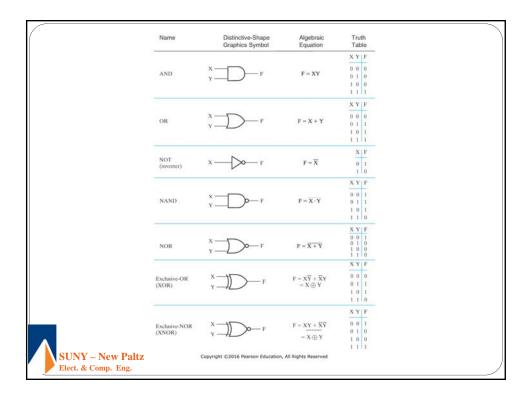
				В	B ₆ B ₅			
B ₄ B ₃ B ₂ B ₁	000	001	010	011	100	101	110	111
0000	NULL	DLE	SP	0	@	P		р
0001	SOH	DC1	!	1	A	Q	a	q
0010	STX	DC2		2	В	R	b	r
0011	ETX	DC3	#	3	C	S	c	S
0100	EOT	DC4	\$	4	D	T	d	t
0101	ENQ	NAK	%	5	E	U	e	u
0110	ACK	SYN	&	6	F	V	f	v
)111	BEL	ETB		7	G	W	g	w
1000	BS	CAN	(8	H	X	h	x
1001	HT	EM)	9	I	Y	i	y
1010	LF	SUB	spr	:	J	Z	j	Z
1011	VT	ESC	+	;	K	[k	{
100	FF	FS	,	<	L	1	1	1
1101	CR	GS	_	=	M]	m	}
110	SO	RS	2	>	N	^	n	~
111	SI	US	/	?	O	100	O	DEL

		$\mathbf{B}_{7}\mathbf{B}_{6}\mathbf{B}_{5}$						
B ₄ B ₃ B ₂ B ₁	000	001	010	011	100	101	110	111
Control Ch	aracters							
NULL	NULL	G			DLE	Data li	nk escape	
SOH	Start of heading			DC1	Device control 1			
STX	Start of text			DC2	Device control 2			
ETX	End of text			DC3	Device	control 3		
EOT	End of	transmiss	ion		DC4	Device	control 4	
ENQ	Enquir	ry			NAK	Negati	ve acknow	ledge
ACK	Ackno	wledge			SYN	Synchr	onous idle	
BEL	Bell				ETB	End of	transmissi	on block
BS	Backsp	pace			CAN	Cancel	l	
HT	Horizo	ntal tab			EM	End of	medium	
LF	Line fe	eed			SUB	Substit	tute	
VT	Vertica	al tab			ESC	Escape	2	
FF	Form f	eed			FS	File se	parator	
CR	Carria	ge return			GS	Group	separator	
SO	Shift o	ut			RS	Record	dseparator	
SI	Shift in	1			US	Unit se	eparator	
SP	Space				DEL	Delete		

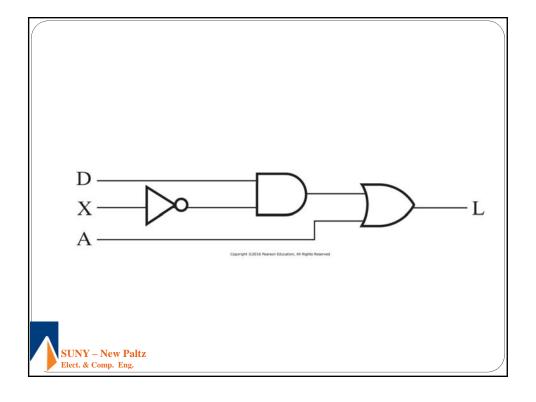








D	Х	Α	L
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
	1	1	1



□ TABLE 2-2 Verilog Primitives for Combinational Logic Gates

Gate primitive	Example instance
and	and (F, X, Y);
or	or (F, X, Y);
not	not (F, Y);
nand	nand $(F, X, Y);$
nor	nor (F, X, Y);
xor	xor (F, X, Y);
xnor	xnor(F, X, Y);

```
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Elect. & Comp. Eng.
```

```
module fig2_5 (L, D, X, A);
input D, X, A;
output L;
wire X_n, t2;

not (X_n, X);
and (t2, D, X_n);
or (L, t2, A);
endmodule

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Elect. & Comp. Eng.
```

☐ TABLE 2-6

Basic Identities of Boolean Algebra

- 1. X + 0 = X
- 2. $X \cdot 1 = X$
- 3. X + 1 = 1
- 4. $X \cdot 0 = 0$
- 5. X + X = X
- 6. $X \cdot X = X$
- 7. $X + \overline{X} = 1$
- 8. $X \cdot \overline{X} = 0$

9. $\overline{\overline{X}} = X$

- 10. X + Y = Y + X
- 11. XY = YX

Commutative

- 12. X + (Y + Z) = (X + Y) + Z 13. X(YZ) = (XY)Z
 - 15. X + YZ = (X + Y)(X + Z) Distributive

Associative

- $14. \quad X(Y+Z)=XY+XZ$ 16. $\overline{X} + \overline{Y} = \overline{X} \cdot \overline{Y}$
- 17. $\overline{X \cdot Y} = \overline{X} + \overline{Y}$
- DeMorgan's



■ TABLE 2-7 Truth Tables to Verify DeMorgan's Theorem

(a) X	Υ	X + Y	$\overline{X} + \overline{Y}$	(b) X	Υ	$\overline{\mathbf{X}}$	Y	$\overline{X} \cdot \overline{Y}$
0	0	0	1	0	0	1	1	1
0	1	1	0	0	1	1	0	0
1	0	1	0	1	0	0	1	0
1	1	1	0	1	1	0	0	0

